Z80 timings on Amstrad CPC - Cheat sheet

This document is a visual layout made by cpcitor/findyway from data at http://www.cpctech.org.uk/docs/instrtim.html

Instruction timings

The main clock in the CPC is 16Mhz This is provided to the Gate-Array which generates the other clocks.

The Gate Array has the following roles:

generation of a 1Mhz clock for the CRTC and AY-3-8912

generation of a 4Mhz clock for the CPU

arbitrates access to the RAM between the CPU and the video hardware (CRTC and Gate-Array)

Every microsecond:

The CRTC generates a memory address using it's MA and RA signal outputs

The Gate-Array fetches two bytes for each address

The video hardware is given priority so that the display is not disrupted

The Gate-Array generates the "READY" signal which is connected to the "/WAIT" input signal of the CPU. This signal is used to stop the CPU accessing while the video-hardware is accessing it. As a result, all instruction timings are stretched so that they are all multiples of a microsecond (1µs), and this gives an effective CPU clock of 3.3Mhz.

Key:	
cc	condition code (z,nz,c,nc,p,m,po,pe)
r	8-bit register (B,C,D,E,H,L,A)
b	Bit number (0,1,2,3,4,5,6,7)
n	8 bit value
nnnn	16 bit value
dd	8 bit displacement
rp	16-bit register (HL,DE,BC) or SP (except for PUSH and POP)
nc	condition not satisfied
c	condition satisfied

Other timings

Time between acknowledge of a interrupt and execution of a interrupt

Mode 0: (depends on instruction)

Mode 1: 5

Mode 2: 19

1 monitor scanline: 64 microseconds

1 50Hz monitor frame: 19968 microseconds.

NOTES:

(note 1) This timing applies when there are multiple DD or FD prefix's together.

The timings for IY index register pair are identical to the timings for IX register pair.

The table on next page gives the complete execution time for all CPU instructions

These timings have been measured

1 NOP	2 NOPs			3 NOPs			4 NOPs		5 NOPs		6 NOPs		7 NOPs
ARITHMETIC & LOGIC													
ADD A,r	ADD A,(HL)	ADD A,HIX	ADD A,n	ADD HL,rp			ADD IX,rp	SBC HL,rp	ADD A,(IX+dd)				
ADC A,r	ADC A,(HL)	ADC A,HIX	ADC a,n					ADC HL,rp	ADC A,(IX+dd)	CPD			
SUB r	SUB A,(HL)	SUB HIX	SUB n						SUB (IX+dd)				
SBC A,r	SBC A,(HL)	SBC A,HIX	SBC A,n						SBC A,(IX+dd)				
AND r	AND (HL)	AND HIX	AND n						AND (IX+dd)				
XOR r	XOR (HL)	XOR HIX	XOR n						XOR (IX+dd)	CPI			
OR r	OR (HL)	OR HIX	OR n						OR (IX+dd)				
CP r	CP (HL)	CP HIX	CP n						CP (IX+dd)				
	RLC r						RLC (HL)						RLC (IX+dd)
RLCA	RRC r						RRC (HL)						RRC (IX+dd)
RRCA	RR r						RR (HL)						RL (IX+dd)
RLA	RL r						RL (HL)						RR (IX+dd)
RRA	SLA r						SLA (HL)		RLD				SLA (IX+dd)
	SLL r						SLL (HL)		RRD				SRA (IX+dd)
	SRL r						SRL (HL)						SLL (IX+dd)
													SRL (IX+dd)
BITS, FLAGS & SPECIAL ARITHMETIC													
SCF	BIT b,r			BIT b,(HL)			RES b,(HL)				BIT r,(IX+dd)		RES r,(IX+dd)
CCF	RES b,r						SET b,(HL)						SET r,(IX+dd)
CPL	SET b,r												
DAA	NEG												
INCR & DECR													
INC r	INC rp	INC HIX	INC LIX	INC (HL)	INC IX								
DEC r	DEC rp	DEX HIX	DEC LIX	DEC (HL)	DEC IX								

LOAD													
LD r,r	LD A,(BC)	LD r,HIX	LD r,n	LD (HL),nn	LD HIX,nn	LD I,A	LD A,(nnnn)	LD IX,nnnn	LD (nnnn),HL	LDI	LD (nnnn),rp		
	LD (BC),A	LD r,LIX			LD LIX,nn	LD A,I	LD (nnnn),A		LD HL,(nnnn)	LDD	LD rp,(nnnn)		
	LD (DE),A	LD HIX,r				LD R,A					(includes LD (nnnn),HL	LD (IX+dd),nn	
	LD A,(DE)	LD LIX,r				LD A,R					and LD (nnnn),HL		
											with ED prefix)		
	LD r,(HL)				LD rp,nnnn				LD r,(IX+dd)			LD (nnnn),IX	
	LD (HL),r								LD (IX+dd),r			LD IX,(nnnn)	
LOAD WITH PC a.k.a. JUMPS													
JP (HL)	JP (IX)			JP nnnn	JR dd		DJNZ dd	b-1=0 : 3, b-1<>0 : 4					
	JR cc,dd	nc : 2, c : 3		JP cc,nnnn	RET		RETN						
							RETI						
PUSH/POP/LOAD WITH SP/CALL/RET													
				POP rp			PUSH rp		CALL nnnn	CALL cc,nnnn			
	LD SP,HL			LD SP,IX				RET cc	PUSH IX	POP IX	EX (SP),HL		EX (SP),IX
								Nc : 2, c : 4	PUSH IY	POP IY			
IN/OUT, SPECIAL													
NOP	ED "nop" (ED 00 - ED 3F)			IN A,(nn)			IN r,(C)		OUTI	IND	LDIR, LDDR	BC-1=0 : 5, BC-1<>0 : 6	
HALT	IM 0			OUT (nn),A			OUT (C),r		OUTD	INI			
EX AF,AF'	IM 1						IN F,(C)				CPDR	BC-1=0 : 5, BC-1<>0 : 6	
EX DE,HL	IM 2						OUT (C),0				CPIR	BC-1=0 : 5, BC-1<>0 : 6	
EXX							RST 0	RST 4					
DI,EI							RST 1	RST 5			INDR, INIR	BC-1=0 : 5, BC-1<>0 : 6	
DD/FD							RST 2	RST 6			OTDR, OTIR		
Prefix (note 1)							RST 3	RST 7					